

A 1.9GHz Wide-Band IF Double Conversion CMOS Integrated Receiver for Cordless Telephone Applications

**Jacques C. Rudell, Jia-Jiunn Ou, Thomas B. Cho*,
George Chien, Francesco Brianti**, Jeffrey A. Weldon,
and Paul R. Gray**

University of California, Berkeley

***San Francisco Telecom / Level 1 Communications**

****SGS Thomson**

Issues in Portable Receiver Design

Commercial portable receiver:

- Low cost
- Small form factors
- Low power

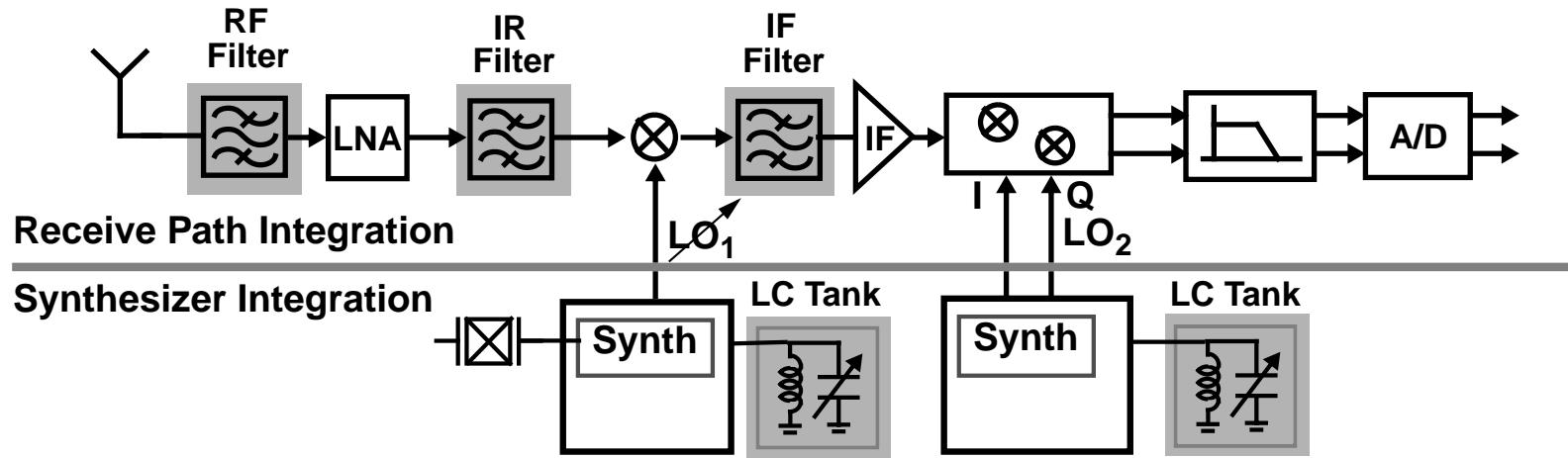
Our highly integrated approach:

- Eliminate the need for external high-Q filters
- Facilitate synthesizer integration
- Potential multi-standard capable features
- Integrate RF blocks in CMOS

Presentation Outline

- Issues in Receiver Integration
- Wide-Band IF with Double Conversion
- CMOS Prototype Description
- Test Results
- Conclusion

Challenges of Receiver Integration



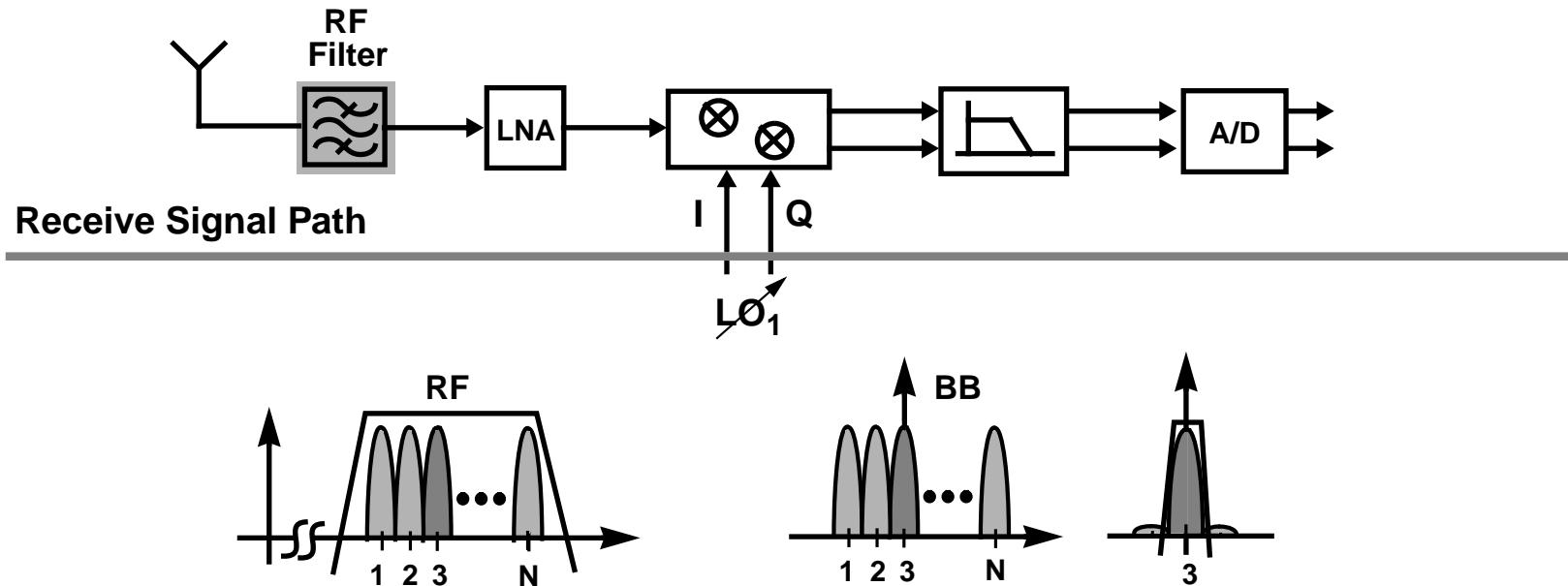
Problems with synthesizer integration:

- Poor phase noise performance of on-chip VCOs
- Channel-select synthesizer required at RF

Challenges in receive path integration:

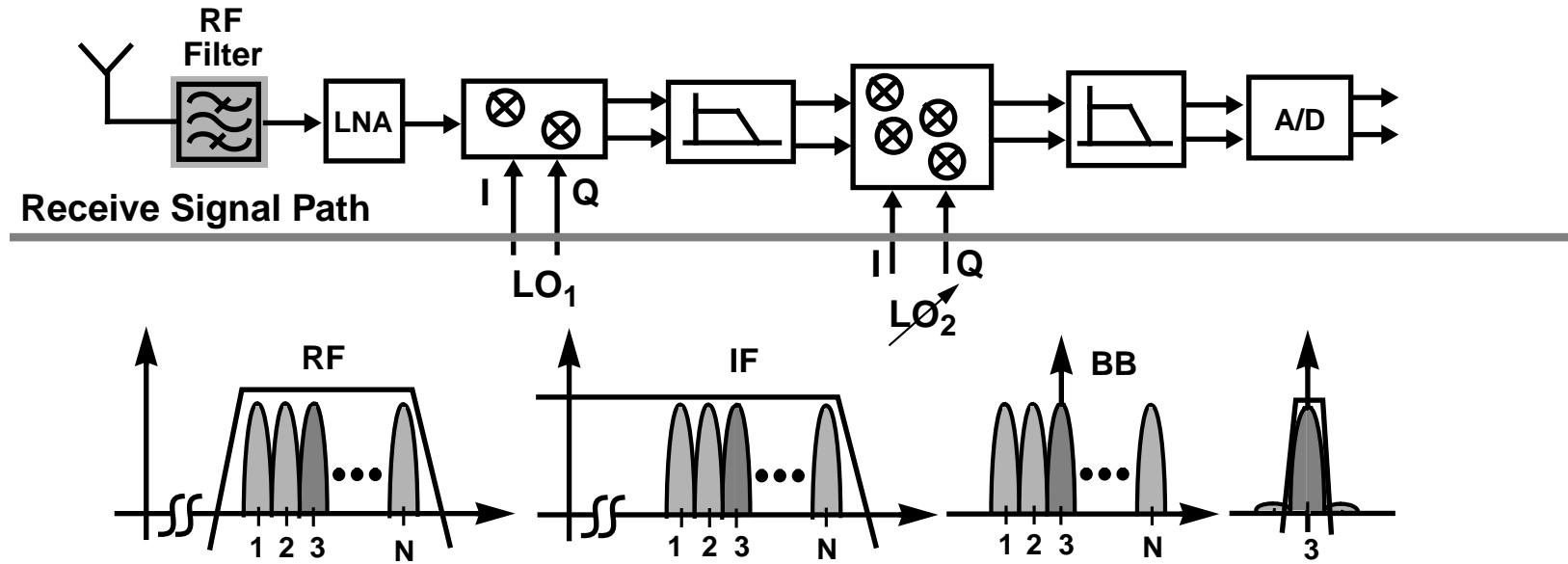
- Image & noise filtering required
- Discrete high-Q IF channel select filter required

Direct Conversion



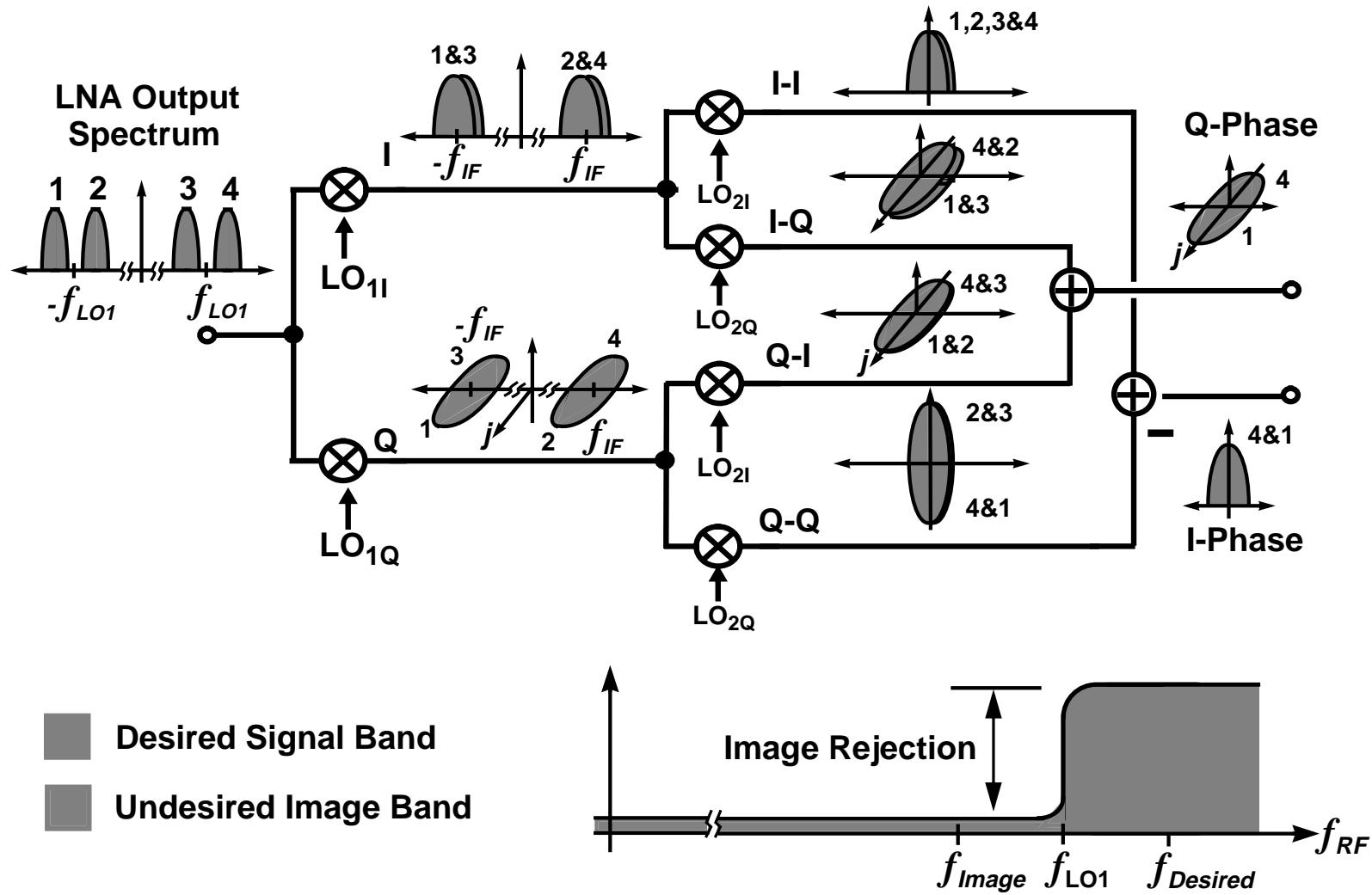
- The need for discrete component filters eliminated
- LO leak creates DC offset
- RF channel-select synthesizer still required

Wide-Band IF w/ Double Conversion



- Channel select filtering performed at baseband
- No LO present at the carrier frequency
- Utilizes IF channel-select synthesizer
- Reintroduces the image problem

Active Image Rejection Technique



Characteristics of WIF

Advantages

- No RF channel-select frequency synthesizer required
- Removes the need for high-Q discrete bandpass filters
- Achieves image rejection without a passive phase shifting filter in the signal path

Disadvantages

- Additional mixers require more power, noise, and distortion
- Image rejection limited by gain matching and LO deviation from quadrature

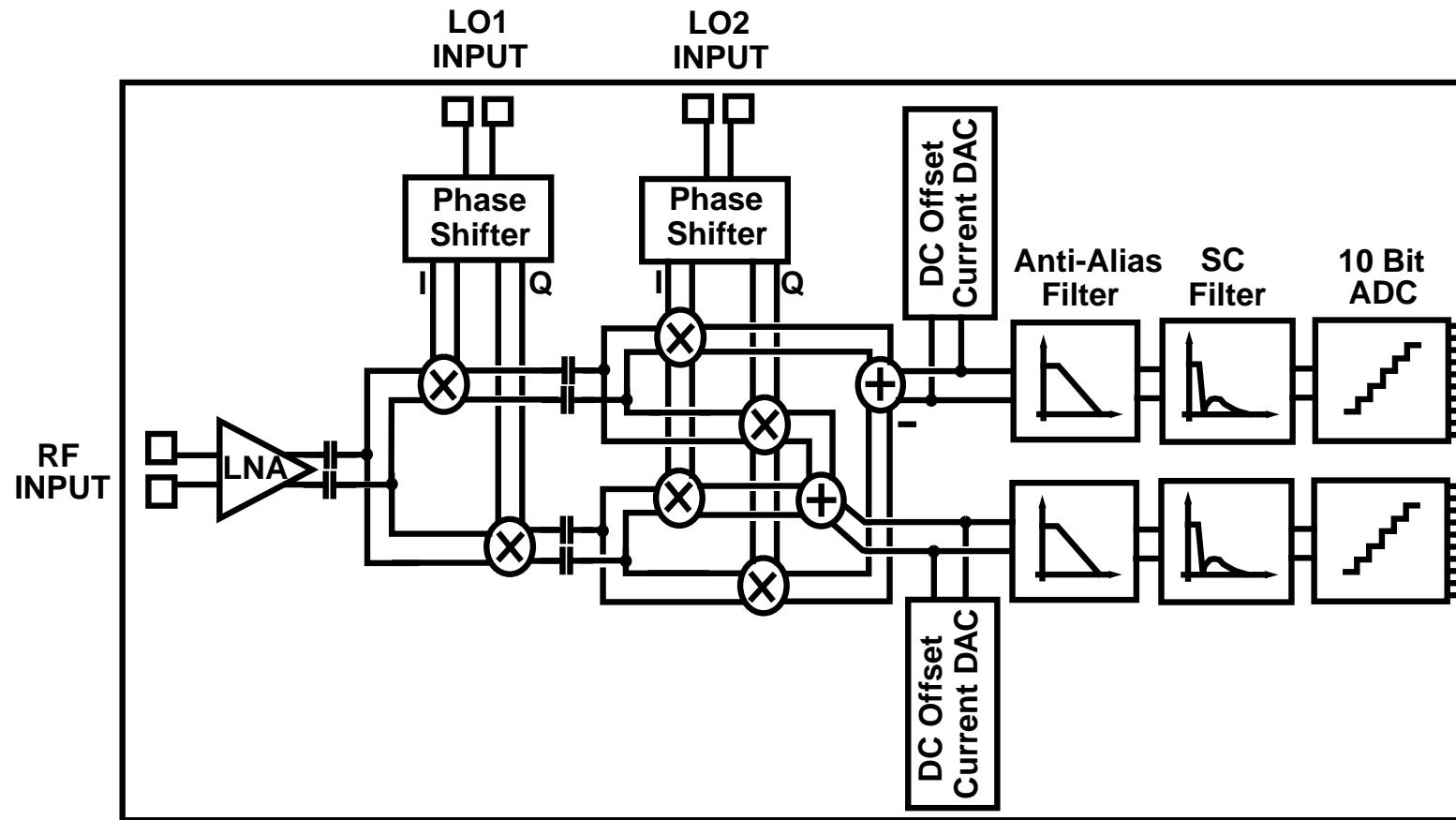
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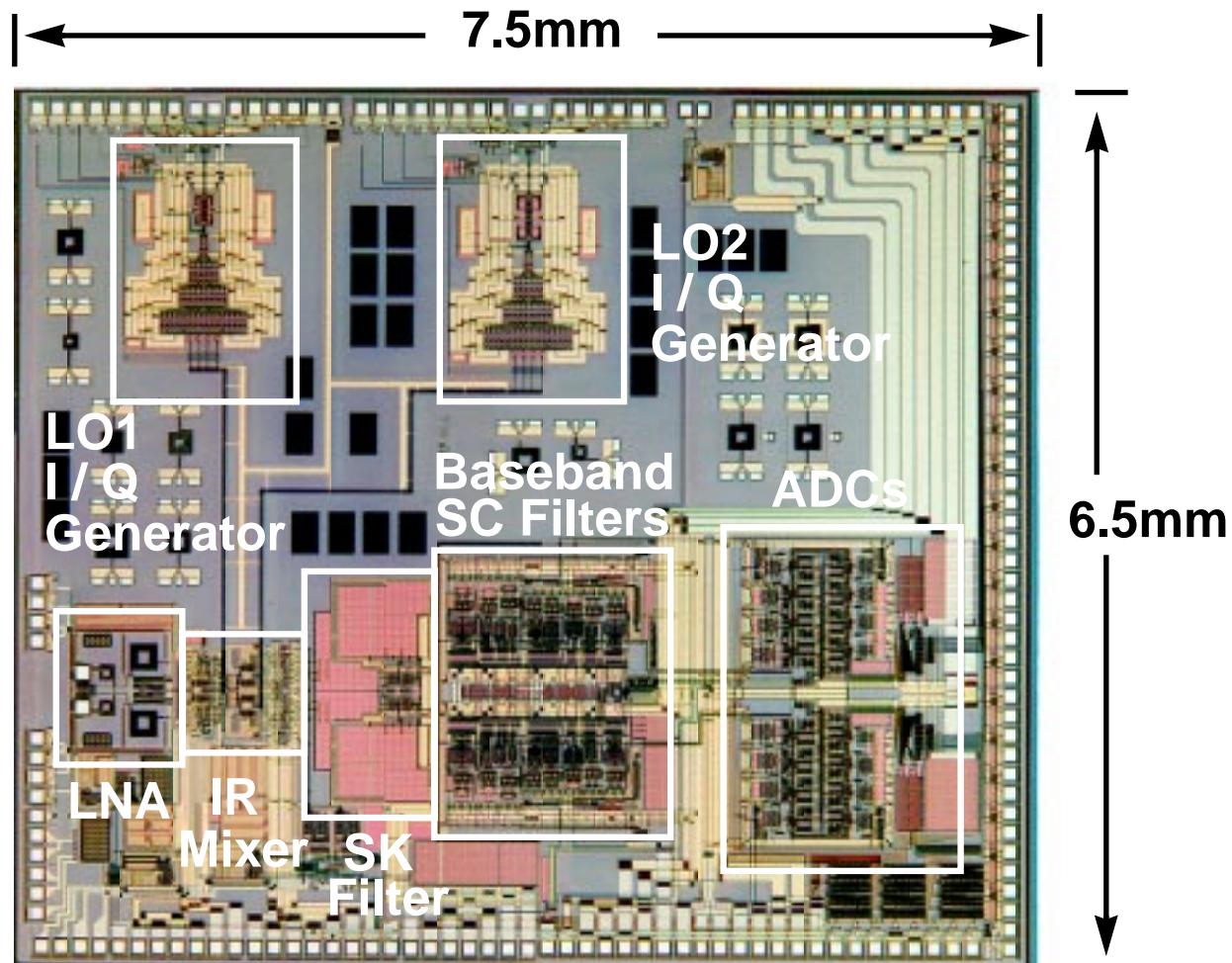
DECT System Specifications

- Digital Enhanced Cordless Telecommunications
- 1.728MHz channel BW; Carrier...1.881GHz to 1.897GHz
- Required reference sensitivity of -83dBm (NF ~ 20dB)
- Greater than -26dBm input-referred IP₃
- GMSK modulation (BT=0.5)
- TDMA / FDMA system

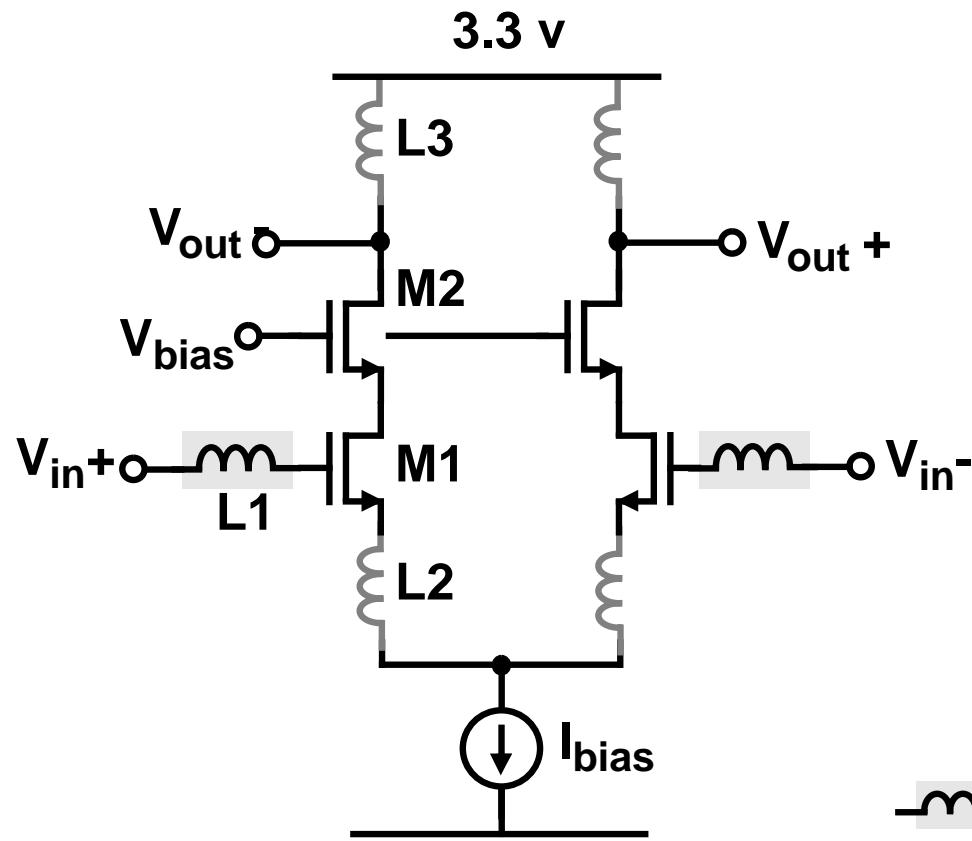
Prototype Block Diagram



Die Photo



Low Noise Amplifier



- Narrowband tuned

- $NF \sim \frac{1}{g_m} \frac{1}{Q^2}$

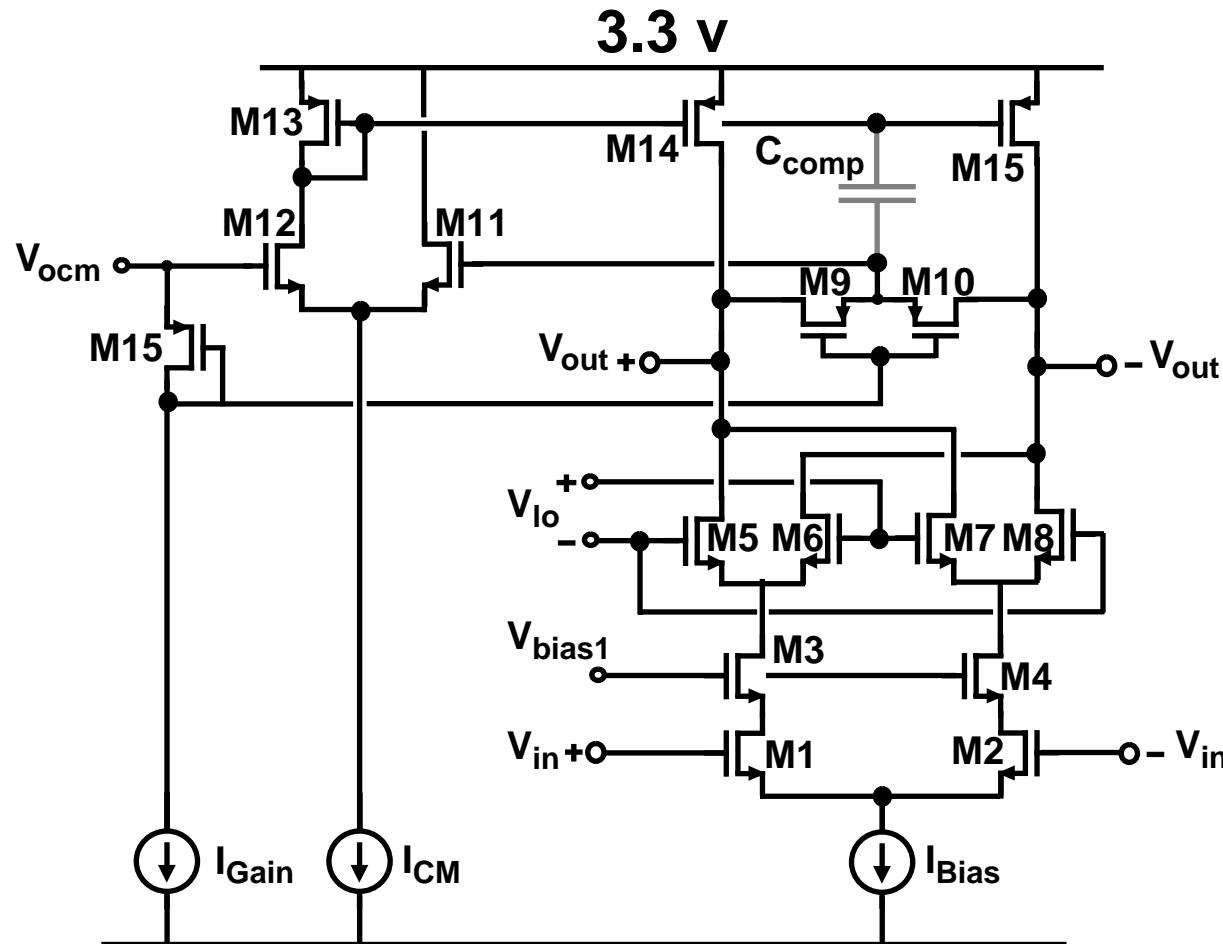
Measured Data

	L2	L3
L (nH)	0.8	6.5
Q@1.9GHz	4	3.7
f _{self} (GHz)	16	3.7

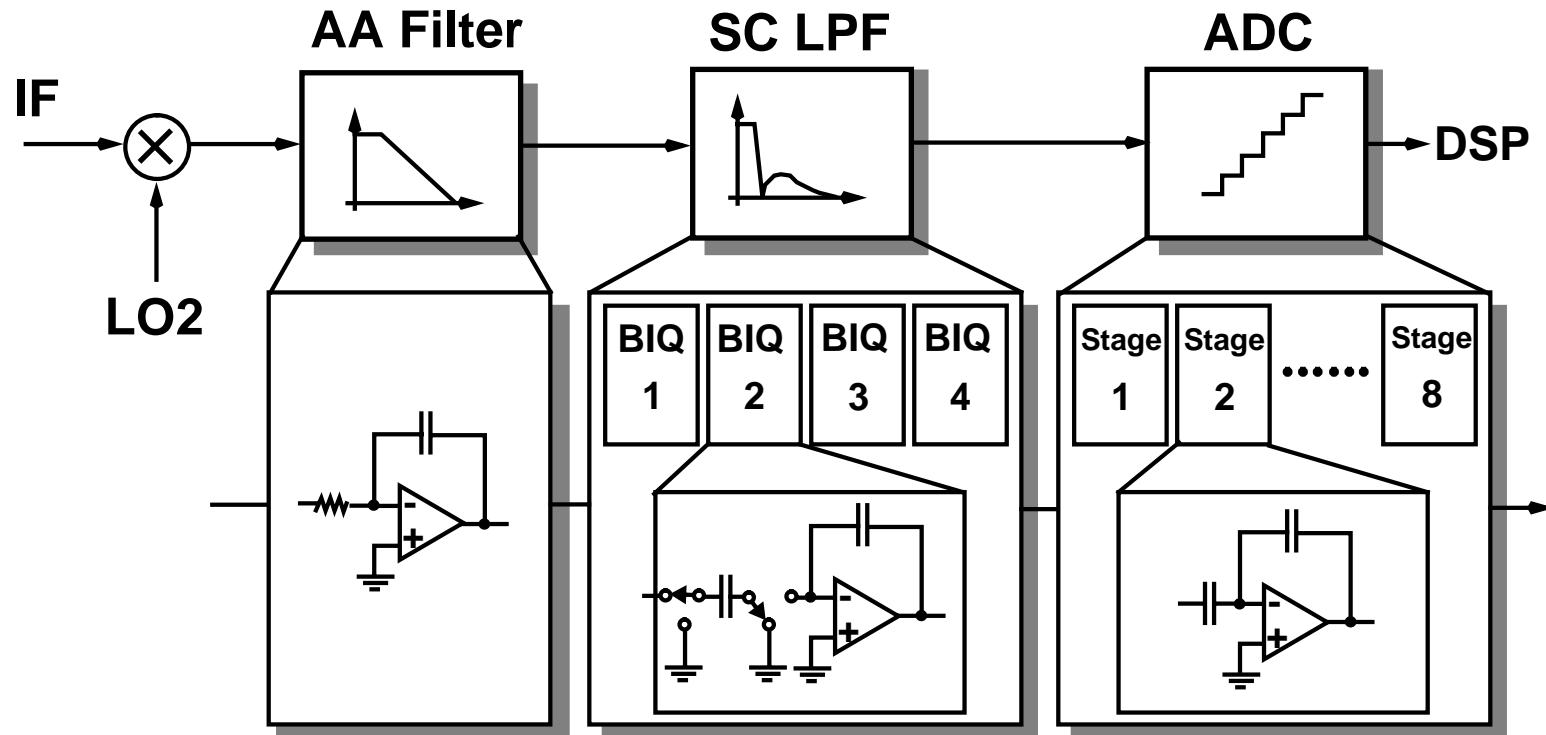
Bondwire Inductors

On-Chip Spiral Inductors

Variable Gain Active Mixer Cell



Baseband Channel Filters



Sallen & Key Filter

- BW = 1.5MHz
- A_v = 6dB

SC filter

- 8th order SC
- A_v = 0 - 42dB
- BW = 700kHz
- f_s = 31.1MS/s

10 Bit Pipeline ADC

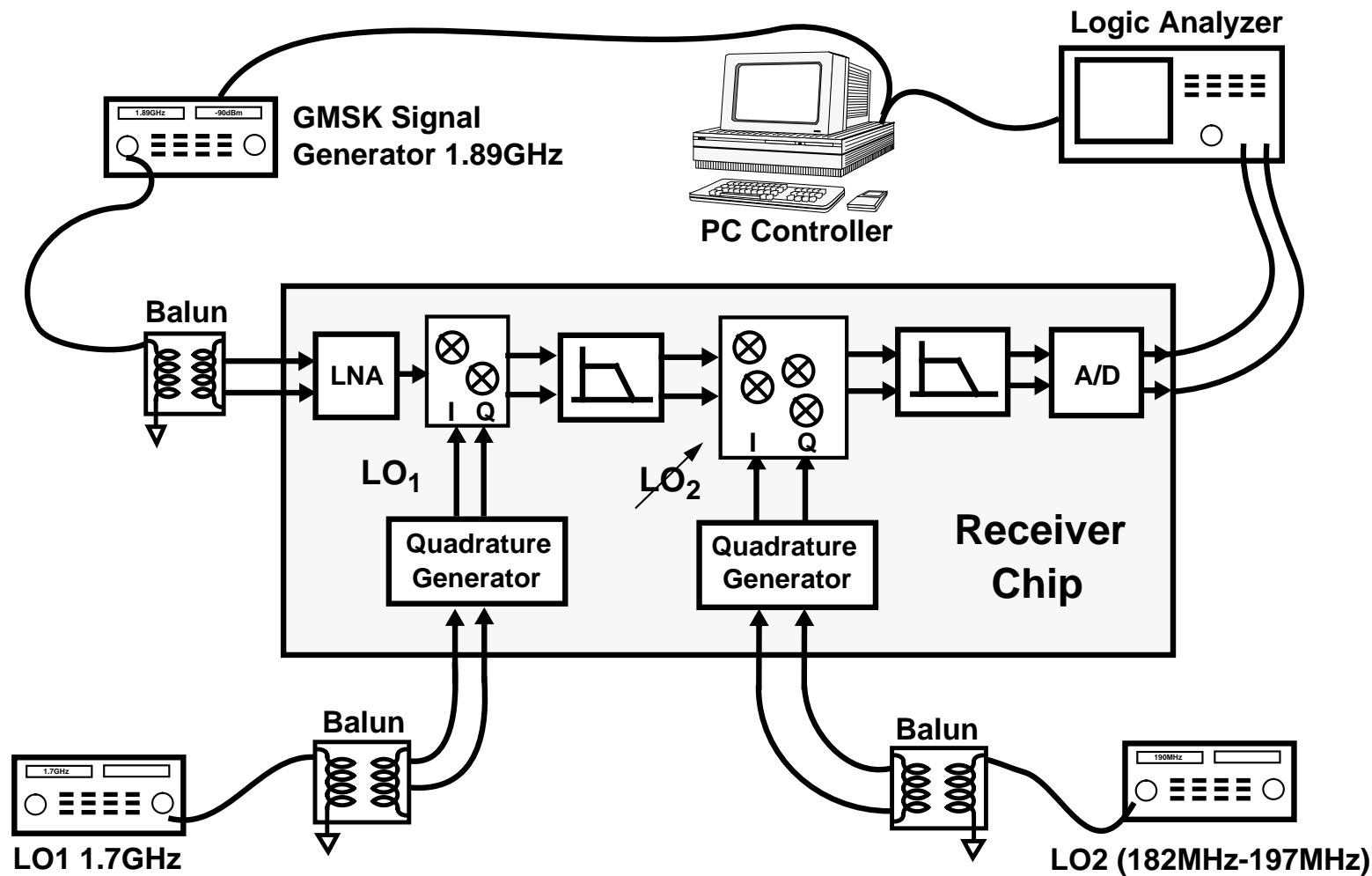
- f_s = 10.3MS/s

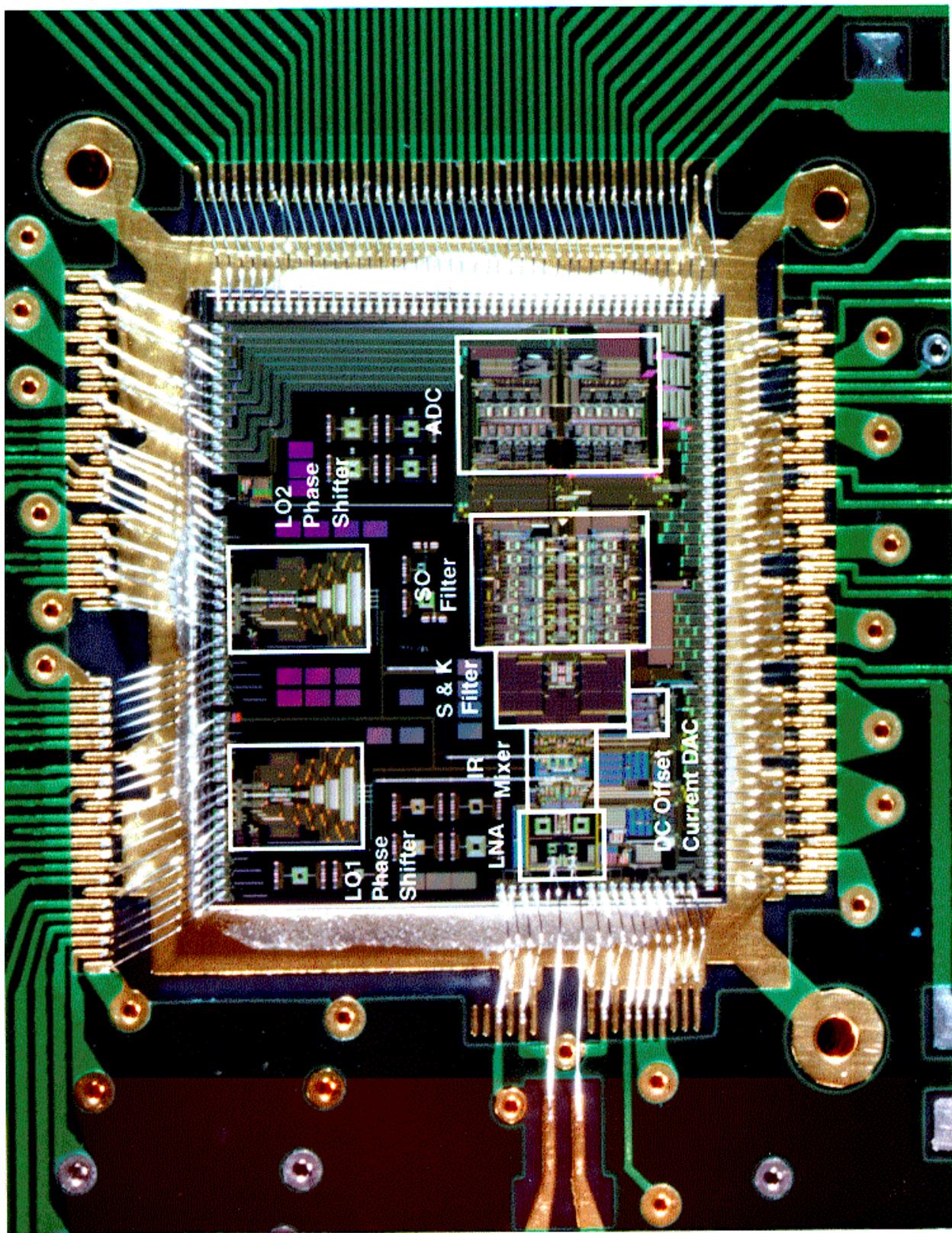
* '96 VLSI Circuit Symp.
T. Cho, et al.

Presentation Outline

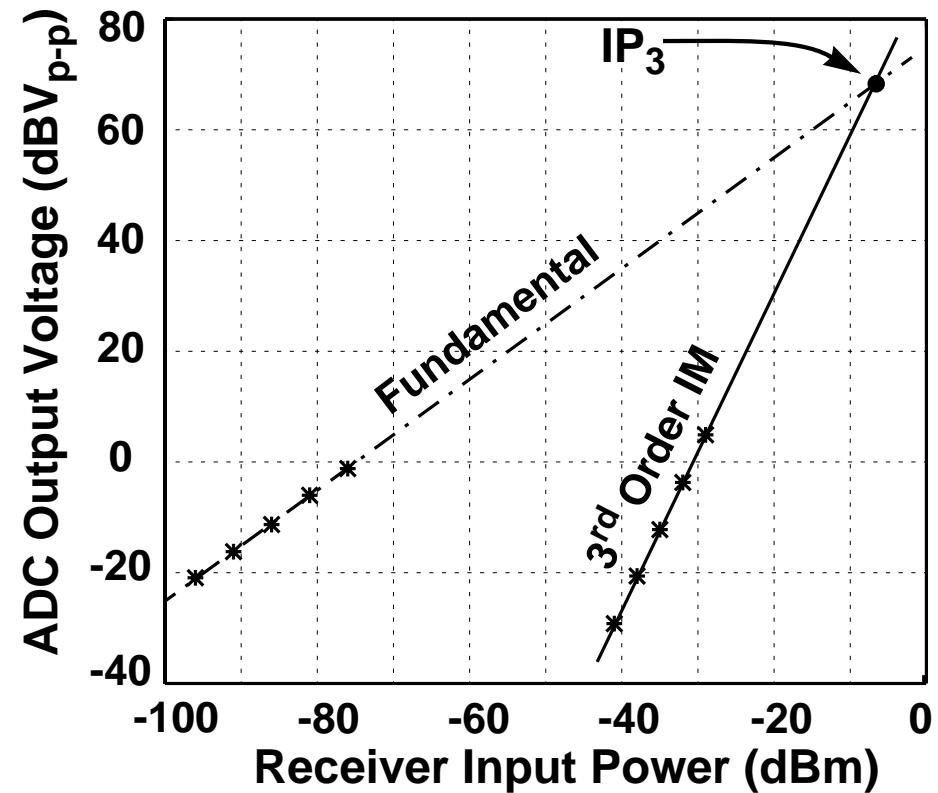
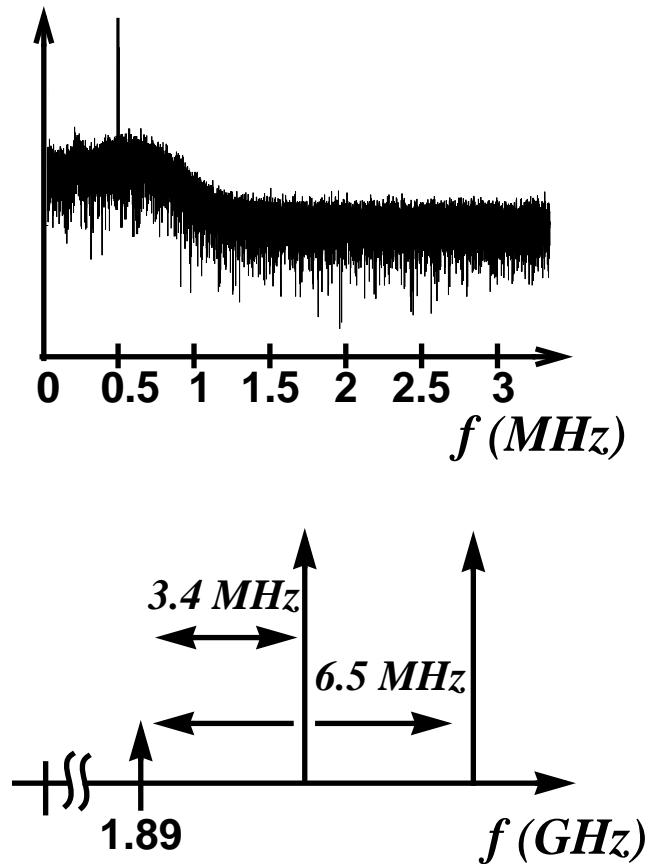
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Receiver Lab Test Setup





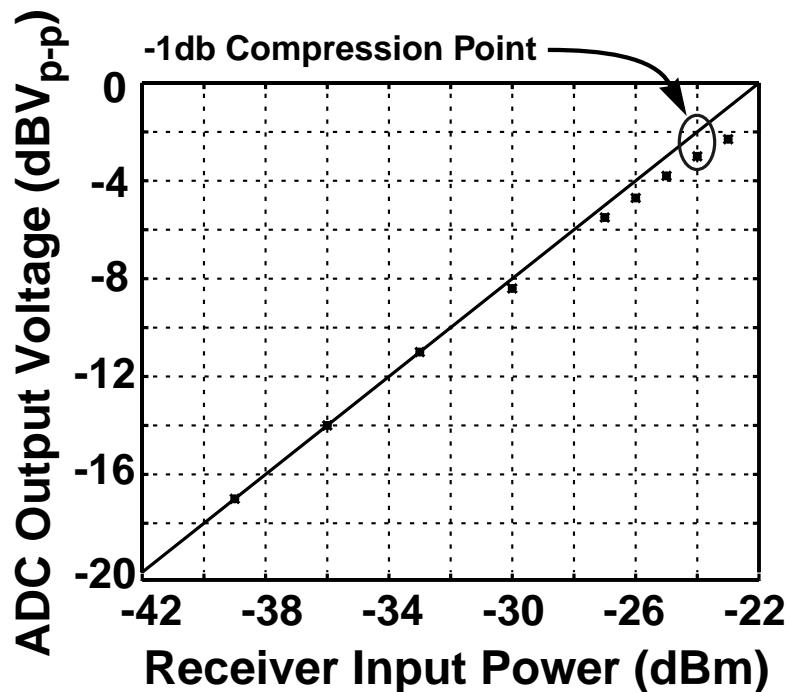
3rd Order Intermodulation



Receiver IP_3 of -7dBm referred to the LNA input

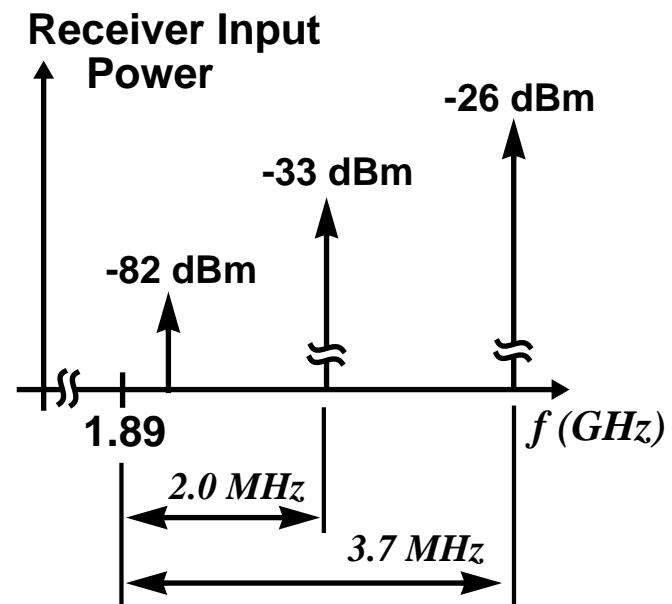
Large Signal Performance

Gain Compression



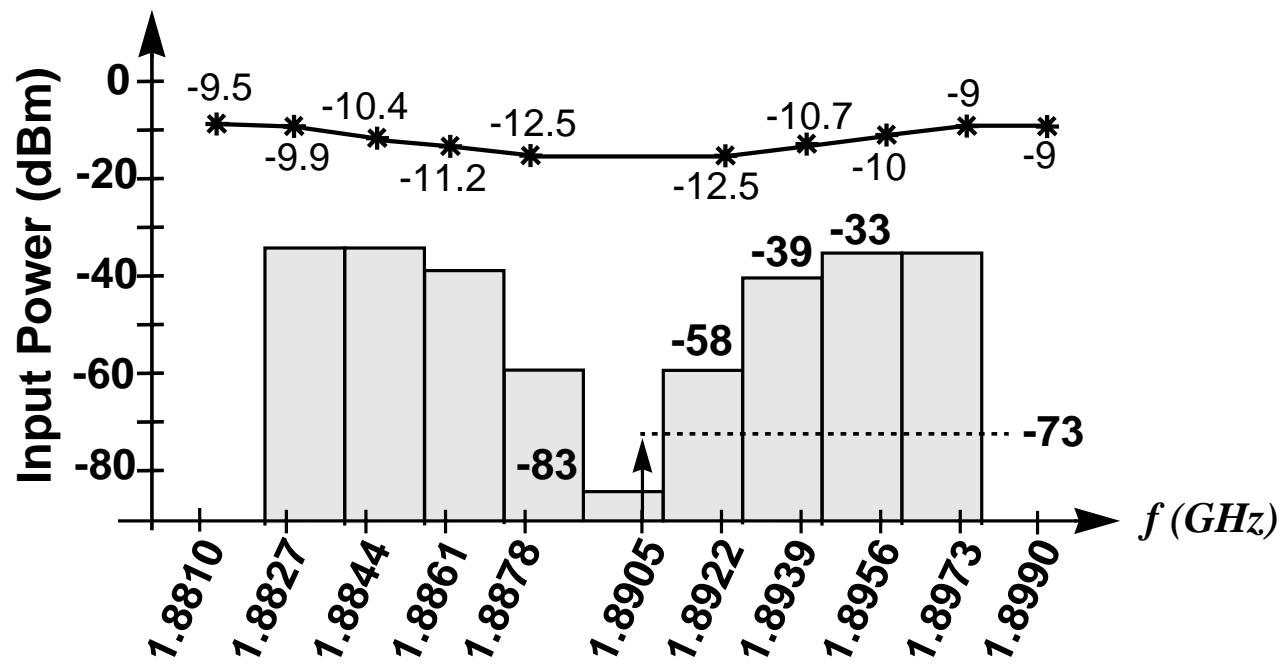
$$P_{-1\text{dB}} = -24 \text{ dBm}$$

Out-of-Band Blocking



$$P_{\text{ob3dB}} = -33 \text{ dBm}$$

Blocking Performance



- DECT blocking requirements.
- * Measured blocker with 10dB CNR for the desired signal.
- ↑ Desired inband signal used for CNR measurement.

Image Suppression

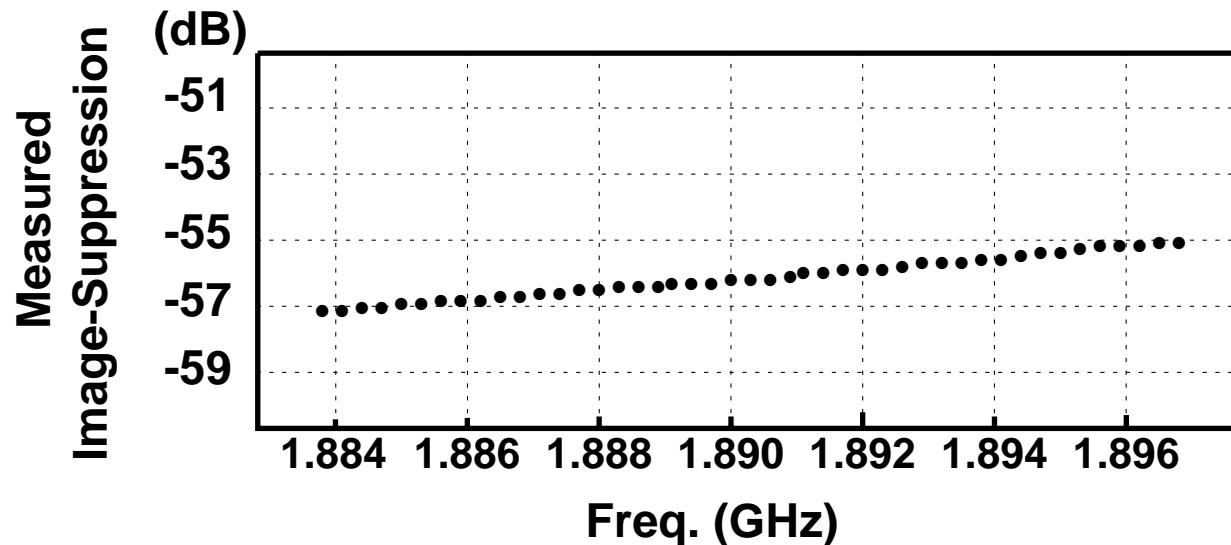


Image-Rejection Contribution

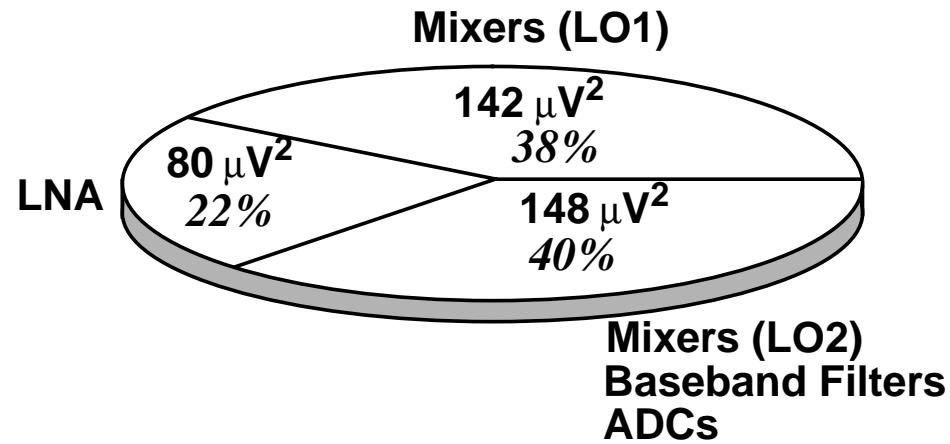
Balun	2dB
LNA	8dB
IR Mixer	45dB
Total IR	55dB

- RF filter provides ~30dB of IR
- Receiver w/ RF filter ~85dB of IR

Noise vs. Power Performance

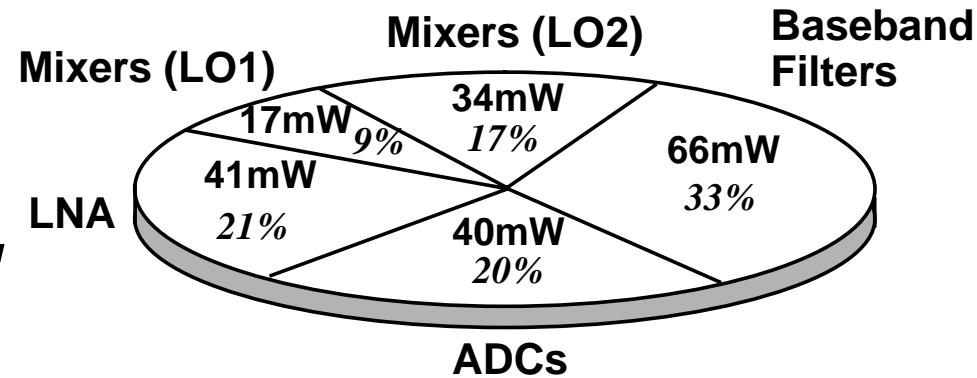
Receiver Sensitivity
-90dBm

Noise Figure
14dB DSB



Total Power Dissipation
198 mW

Power cycled receiver
8% duty cycle = 15.8 mW



Receiver Measured Results

	Prototype	DECT
Sensitivity	-90dBm	-83dBm
Input IP3 (Max. gain setting)	-7dBm	-26dBm
P _{-1dB} (Min gain setting)	-24dBm	-33dBm
Receiver Image Rejection	~85dB w/ RF Filter	~70dB w/ 200MHz IF
P _{ob3dB} (Max. gain setting)	-33dBm @ 2MHz	N/A
Max. Receiver Gain	78dB	N/A
Min. Receiver Gain	26dB	N/A
Active Chip Area	15mm ²	N/A
Power Supply	3.3v	N/A
Silicon Technology	0.6μm DPTM CMOS	N/A

Conclusion

- Phase shifting filters not required by the image-rejection mixer
- Wideband IF w/ Double Conversion Architecture allows:
 - Highly integrated receiver path
 - Relaxed integrated synthesizer requirements
 - Multi-standard capable features
- Feasibility of a highly integrated all-CMOS receiver operating at 1.9 GHz has been demonstrated

Acknowledgments

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